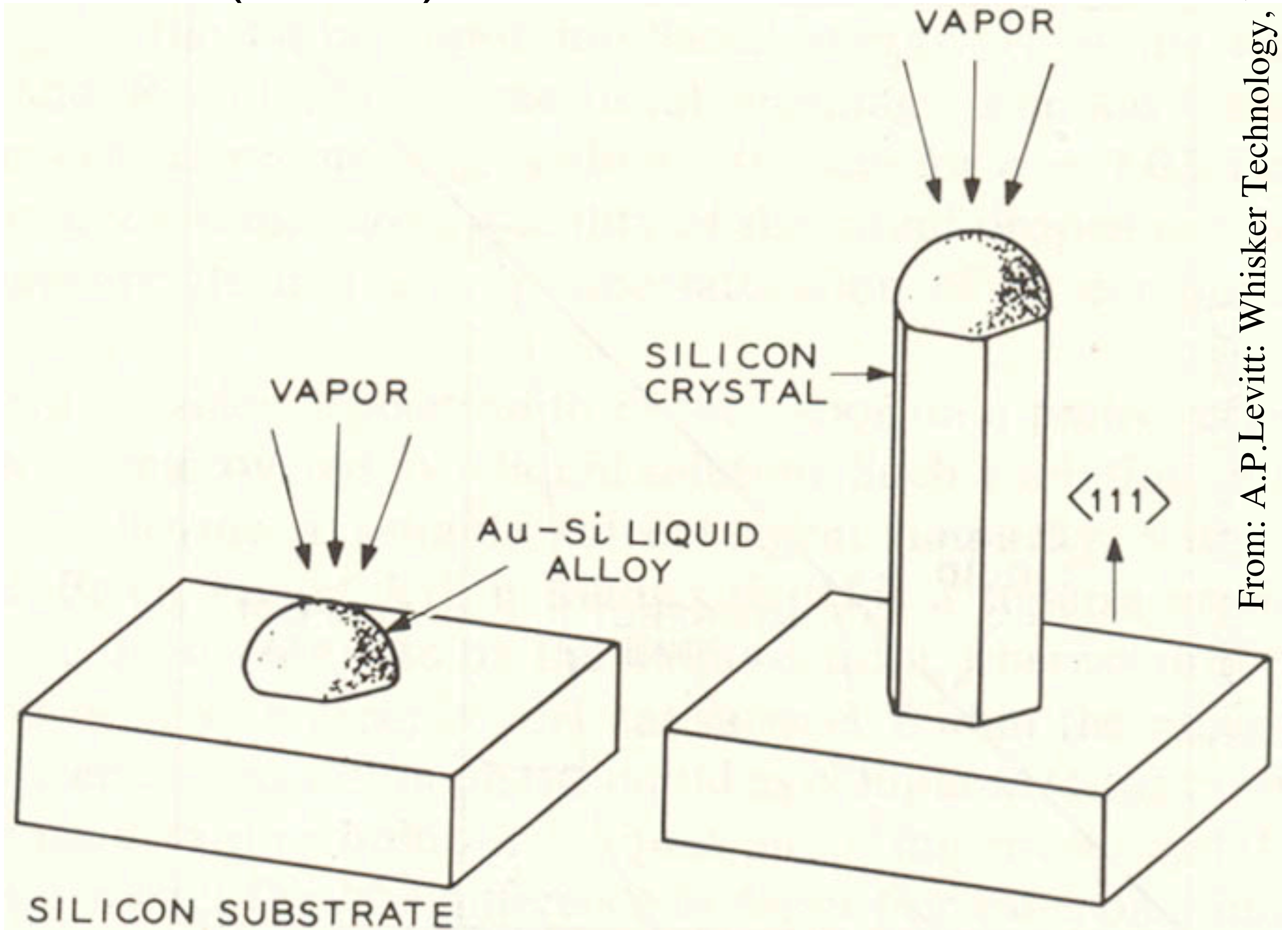
Semiconductor Nanowires: Motivation

- Patterning into sub 50 nm range is difficult with optical lithography. Self-organized growth of nanowires enables 2D confinement of carriers with large splitting of discrete energy states.
- Introduction of heterojunctions between semiconductors with different band gaps allows 3D confinement in sub 50 nm range.
- Room temperature single electron transistors are possible.
- Single photon devices are possible.

"Vapor-Liquid-Solid (VLS)" Growth of Si-Wire

- Si substrate with Au cluster is heated until liquid Au-Si alloy forms
- Si-vapor/Si-precursor impinges on surface and Si gets dissolved in Au-Si liquid supersaturating it
- Si precipitates at liquid/wafer interface
- Wire starts growing while lifting alloy drop up
- Wire assumes same crystal structure as substrate (epitaxial growth)



From: A.P.Levitt: Whisker Technology, Wiley,1970

<u>Questions to answer:</u>

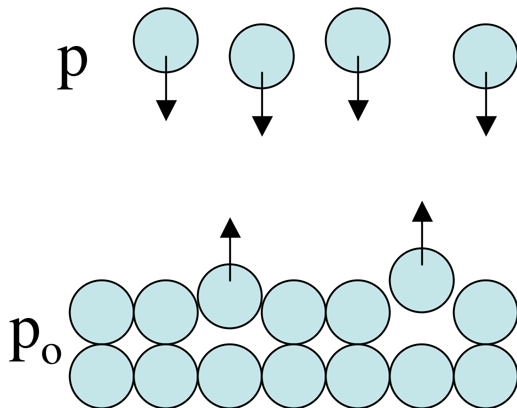
(1) Why does the Si-precursor not deposit on area surrounding the liquid alloy?

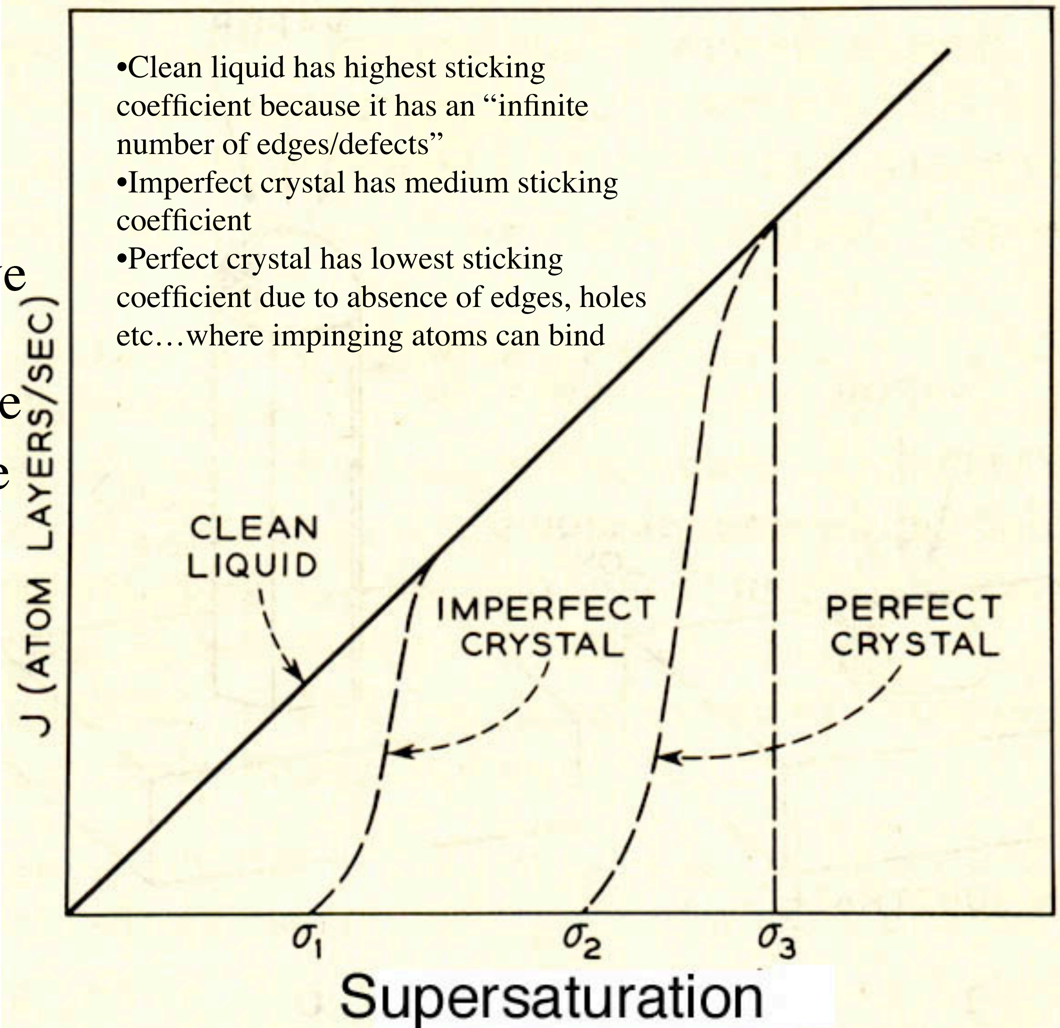
(2) What is going on in the alloy droplet?

(3) Why does the Si precipitate at all?

(1) Growth Rate Vs. Supersaturation/Sticking Coefficient

- Plot shows growth rate J [layers per sec] versus the supersaturation σ.
- J~ σ∗sticking coefficient∗$T^{-1/2}$
- $\sigma = (p-p_o)/p_o$; $p > p_0$ needed for growth
- p=vapor pressure of precursor above surface
- p_o=vapor pressure of sample surface
- Liquid has much higher growth rate below σ_1, i.e. careful adjustment of precursor pressure allows to exclusively absorb precursor atoms in the liquid.





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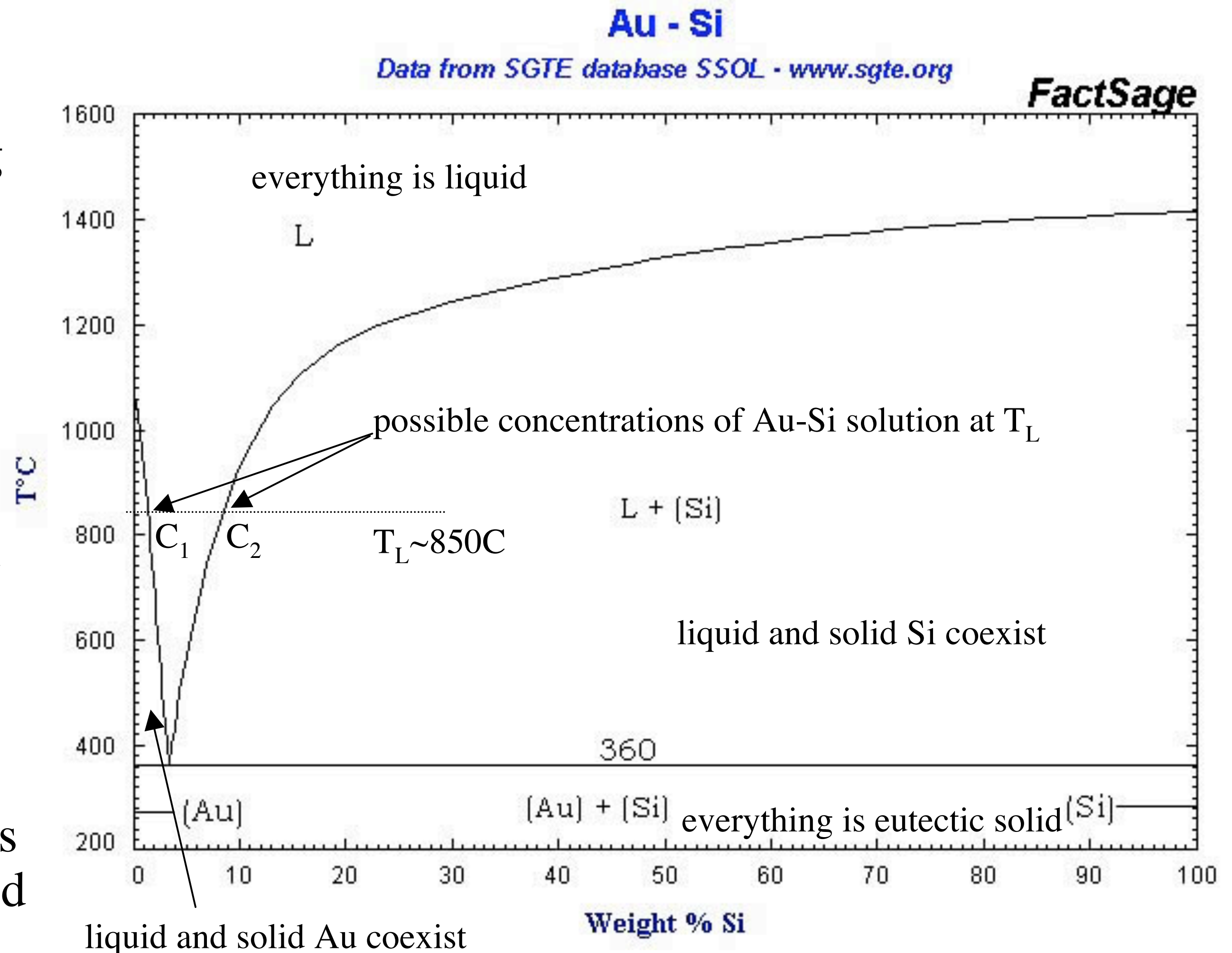
(2,3) Au-Si Phase Diagram: Growth by Supersaturation

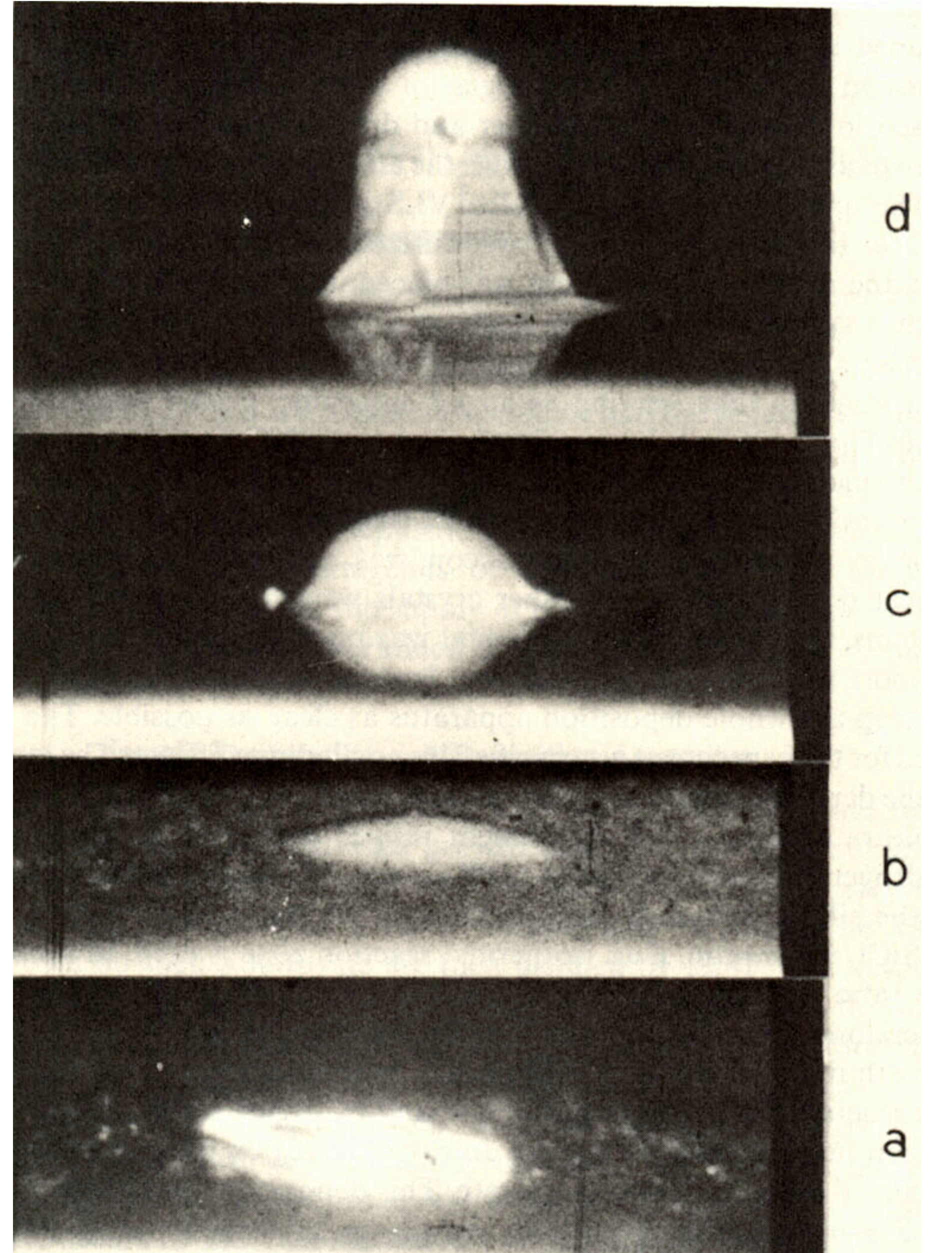
- Au and Si form eutectic mixture (i.e. the mixture can have a lower melting point than the pure materials.
- As the sample is heated, the Au particle on Si-wafer melts and due to "infinite" Si supply a solution of concentration C_2 develops
- As more Si is supplied from gas phase, the solution becomes supersaturated and excess Si precipitates out as solid Si particles which eventually bind to the Si surface under the Au droplet



•Au and Si do not exist in homogenous solution, only as eutectic solid (crystallites of pure Au and Si form a solid body)

Si-Whisker Growth

a) Piece of Au foil lying on Si substrate.
b) Au-Si alloy droplet at 1050C.
c) After 10 min of growth from $SiCl_4$ precursor. Contact angle considerably increases with the consequence of a reduction of the droplet diameter.
d) After 30 min of growth: Contact angle has stabilized and whisker has grown.



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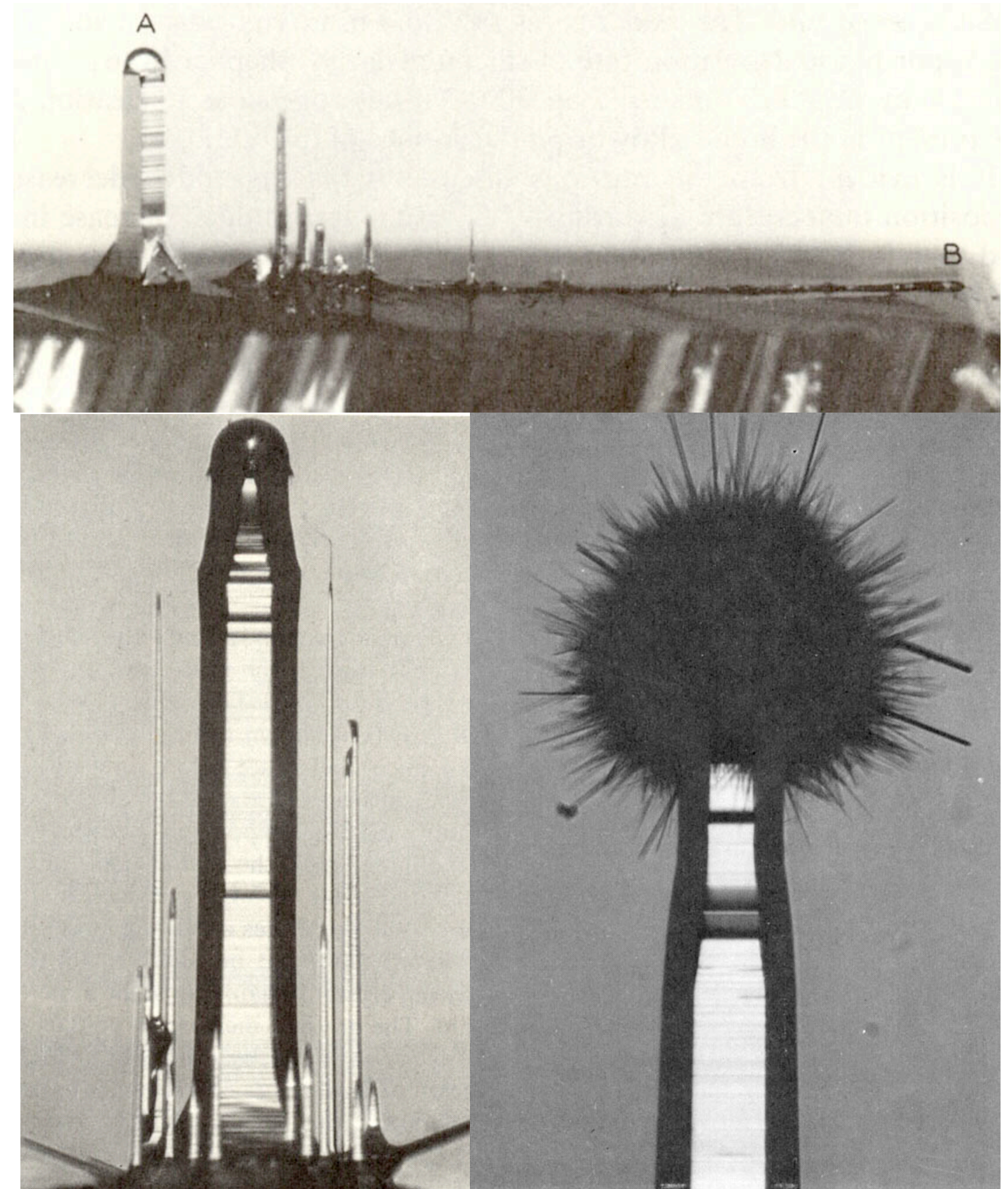
Life is Not Easy: VLS Growth Artifacts

- Top: Temperature gradient on wafer: Alloy droplet originally at A migrates towards higher temp. B.
- Left: Too much precursor vapor results in breakup of original droplet, resulting in smaller whiskers.
- Right: Sudden drop in temperature from 1000C to 600C for 30 sec and subsequent re-heating to 950C resulted in rapid formation of small Si crystals with random orientation serving as seeds for small whiskers.



Size, Shape and Position Controlled GaAs Nanowires

- Size selected Au particles in N_2 stream are deposited on GaAs(111)B surface inside a glove box.
- AFM inside glove box is used to push the Au particles into position.
- Growth occurs at Au particle location using VLS mechanism.
- Precursors: triethylgallium (TEG) and tertiarybutylarsine (TBA). TBA is thermally precracked to release As_2 molecules.

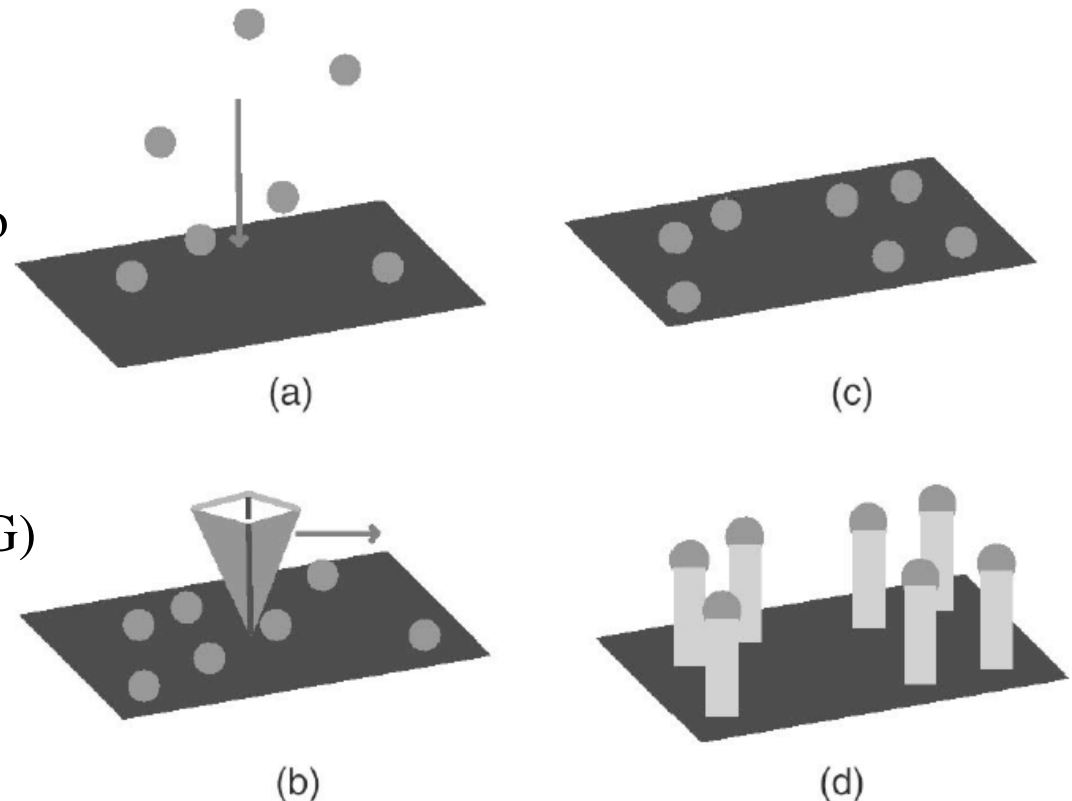
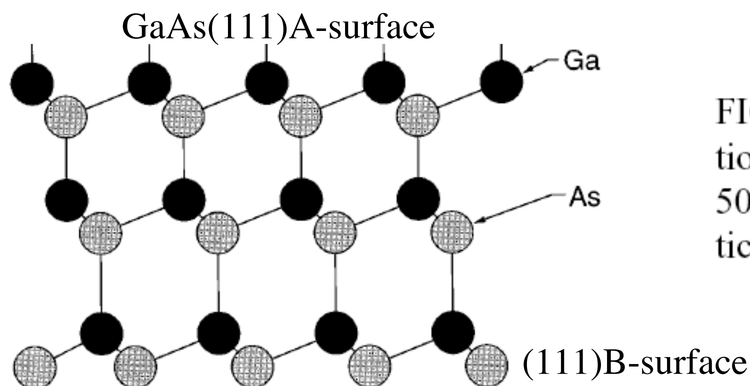


FIG. 1. Schematic depiction of the whisker fabrication process. (a) Deposition of Au aerosol nano-particles, size selected in the range between 10 and 50 nm; (b) optional AFM nano-manipulation of individual Au aerosol particles; (c) annealing step; (d) precipitation, growth of the nano-whiskers.



From: B.J. Ohlson et al., Appl.Phys.Lett. 79(20),pp.3335,2001

Small Particle Mobility Analyzer

- Selects particles of certain mobility (mass) from distribution
- High voltage is applied between center rod and outer wall
- Particles (aerosol, red) enter main gas (air or N_2) stream (blue)and get electrostatically attracted to center rod.
- Only particles of certain mass enter exit hole to “sampling outlet”
- A stream of mono-disperse particles is

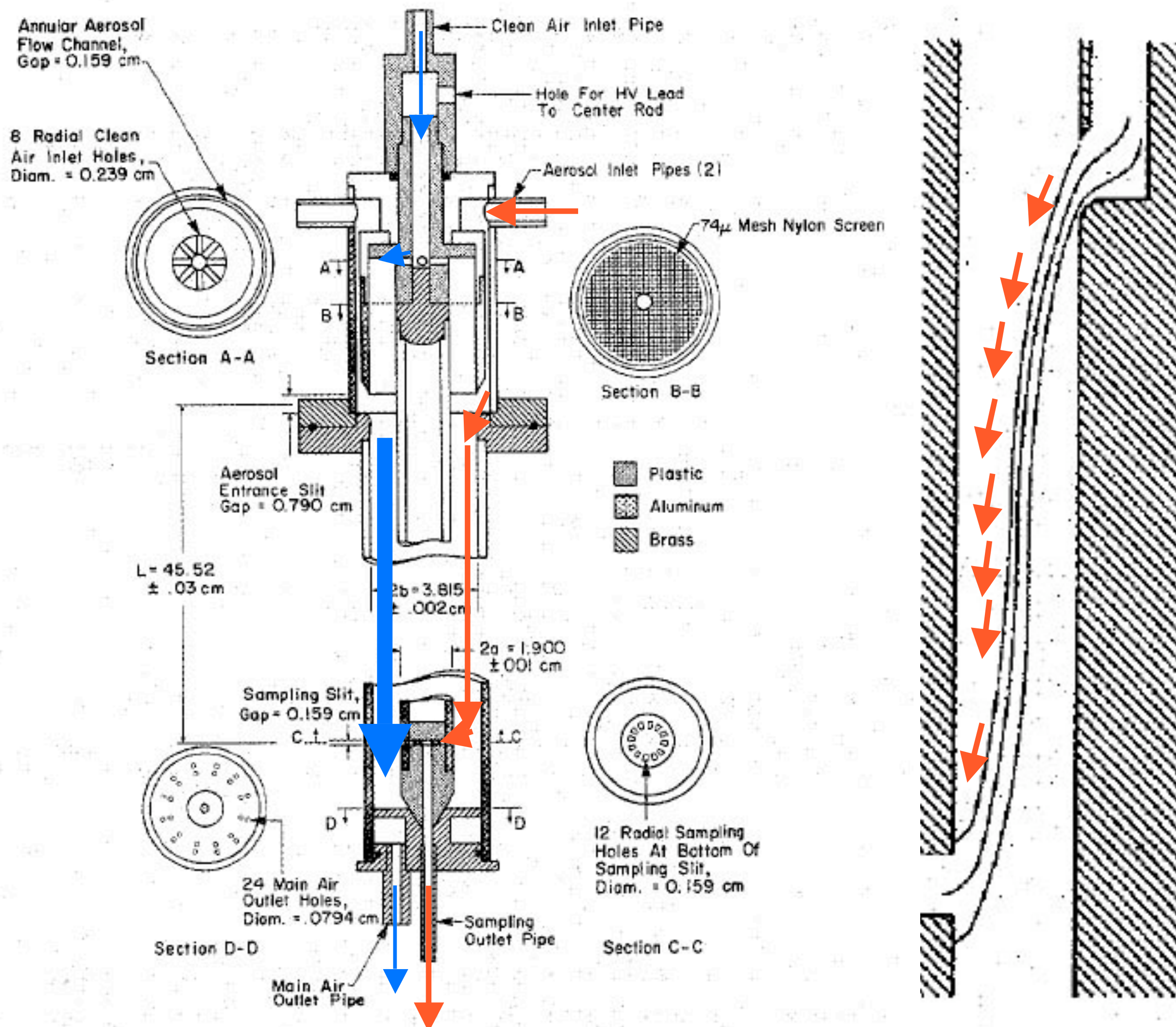
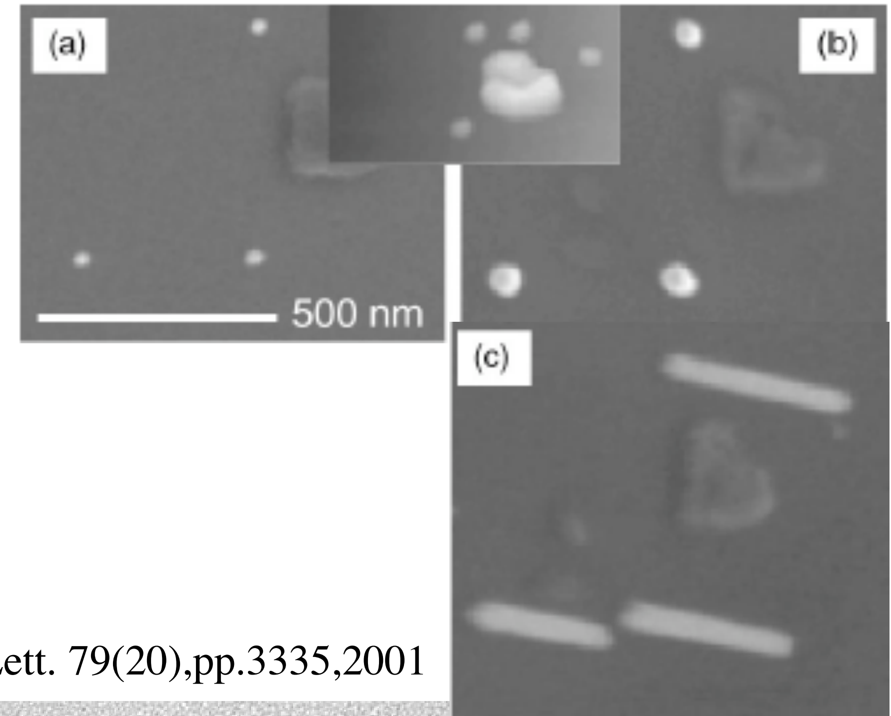


Fig. 1. The mobility analyzer.

From: E.O.Knudson et al., J.Aerosol Sci.,6,pp.443-451,1975

GaAs Nanowires Growth Results

- (top): Au particles moved into growth positions(a), with grown GaAs wires, top view(b), side view(c).
- (bottom): Randomly distributed wires (b), TEM image of wire end (c); Different crystal structures and defects are visible (W=wurzite, Z=zinc blende, SF=stacking fault,T=twin plane). Cap at the end: Au particle.



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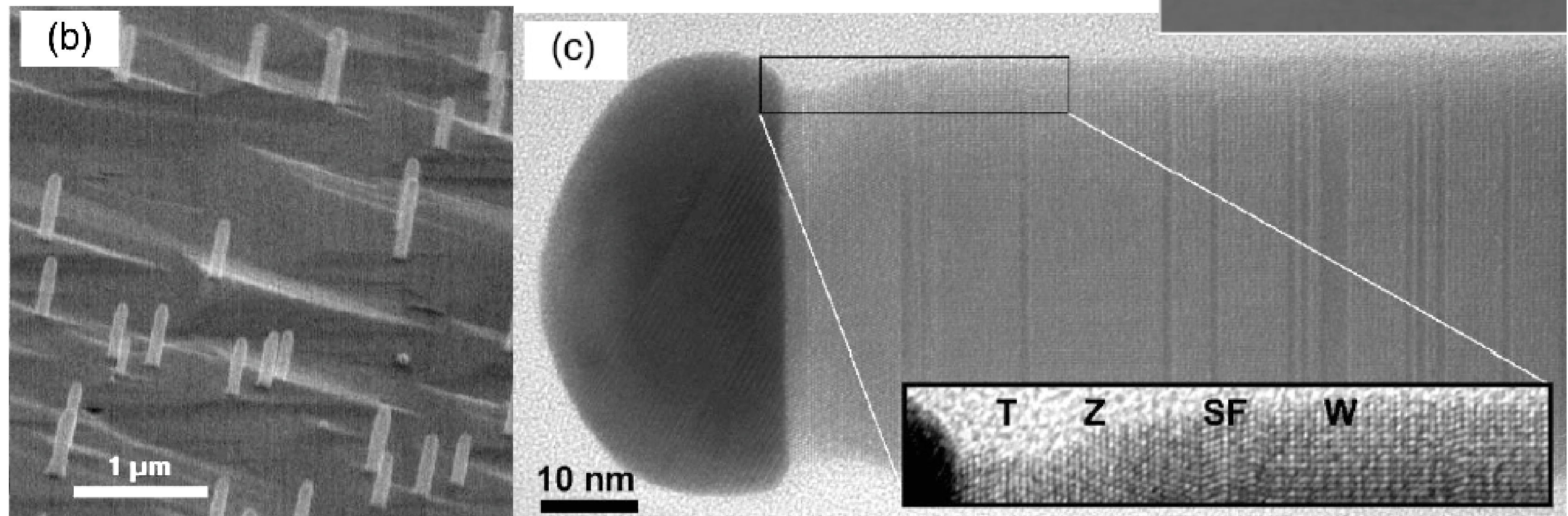
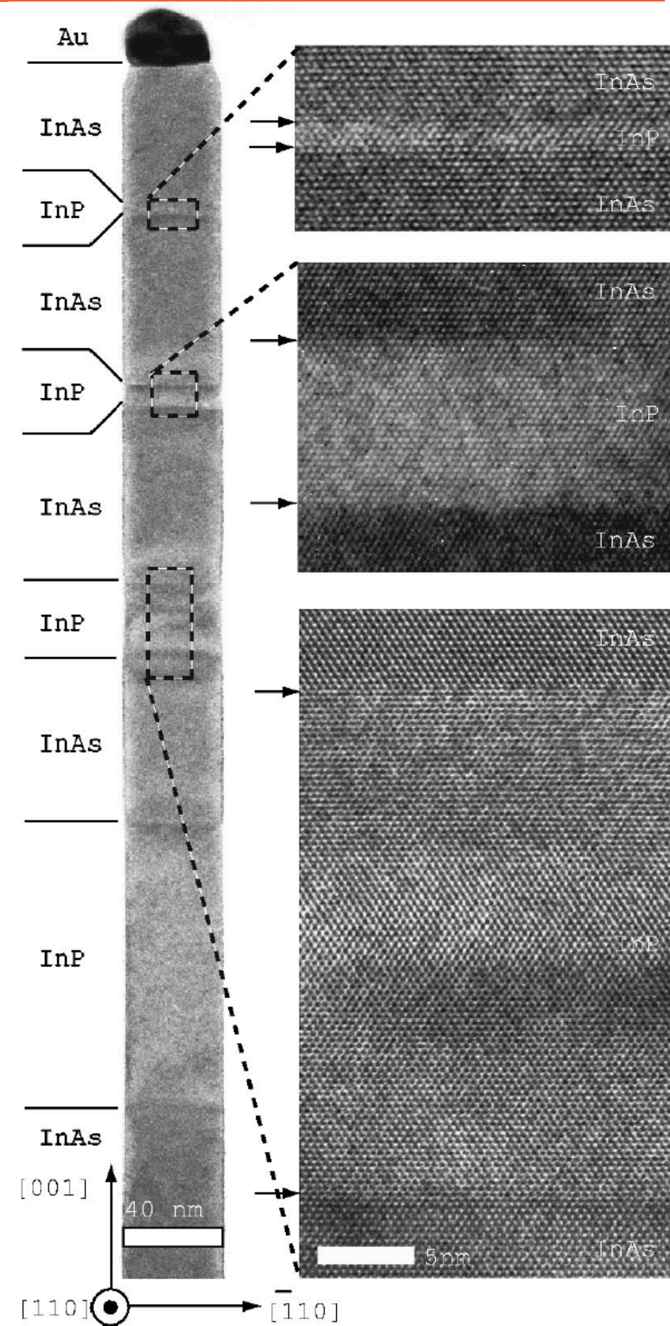


InAs/InP Heterostructure Nanowires

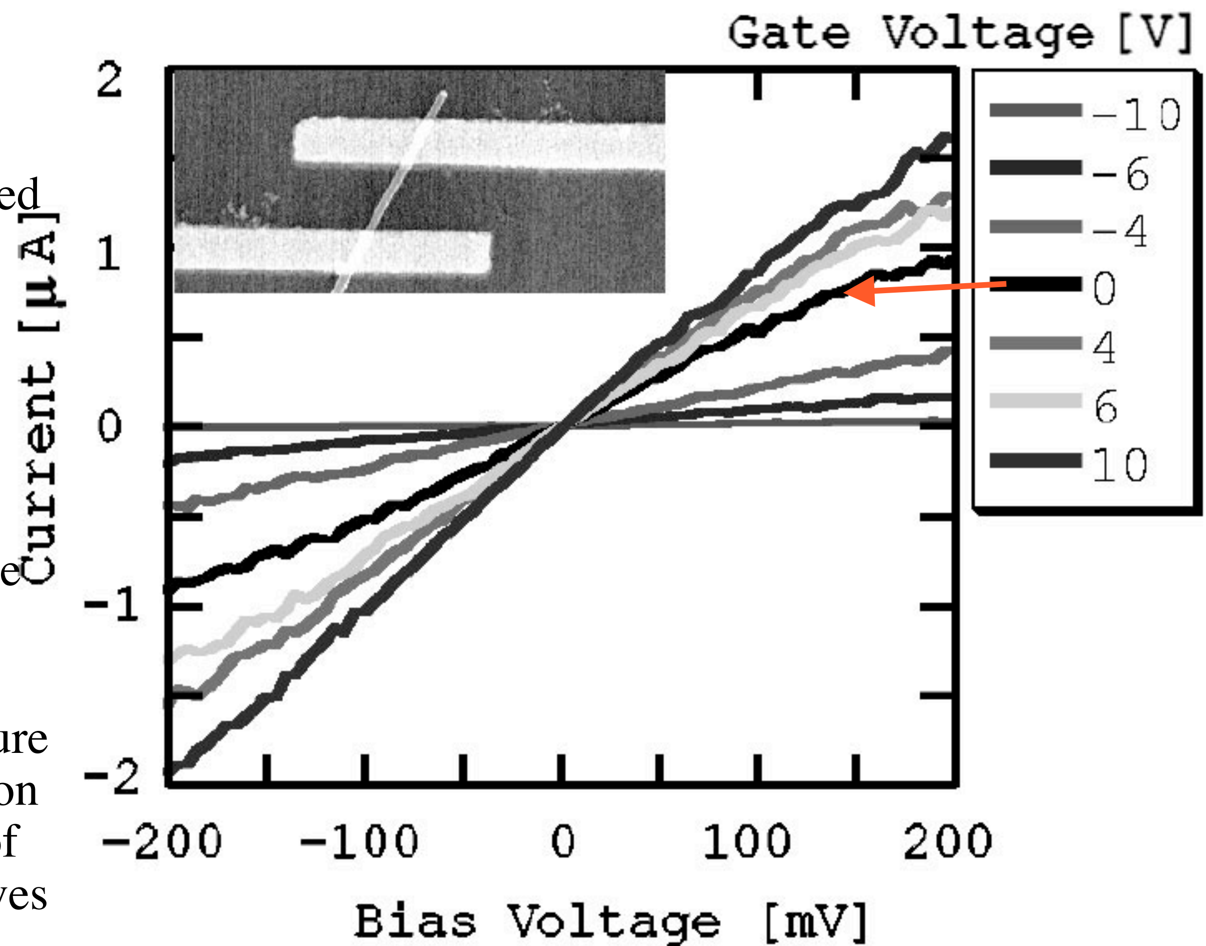
- Same VLS-procedure as for pure wires using trimethyl In, tertiarybutylarsine, and tertiarybutylphosphine as precursors.
- 40 nm width.
- Alternating between arsine and phosphine precursors produces alternating InP and InAs growth regions.
- TEM shows atomically abrupt interfaces.



From: M.T.Björk et al. Appl.Phys.Lett. 80(6),1058,2002

InAs/InP Devices and Their Characterization

- E-beam litho was used to make contacts for electrical characterization.
- Wires were dispersed on oxidized Si wafer (100 nm). Then 20 nm Ni/70 nm Au electrodes were patterned across the ends of the wire.
- Two kinds of wires were fabricated: (1) Pure InAs references and (2) InAs with one 80 nm long InP section in the middle.
- Graph shows current through pure InAs wire (at 4.2K) depending on a bias applied to the back side of the Si wafer(=gate). Linear curves demonstrate Ohmic behavior.
- Conductivity changes strongly due to changing carrier density of wire.



From: M.T.Björk et al. Appl.Phys.Lett. 80(6),1058,2002

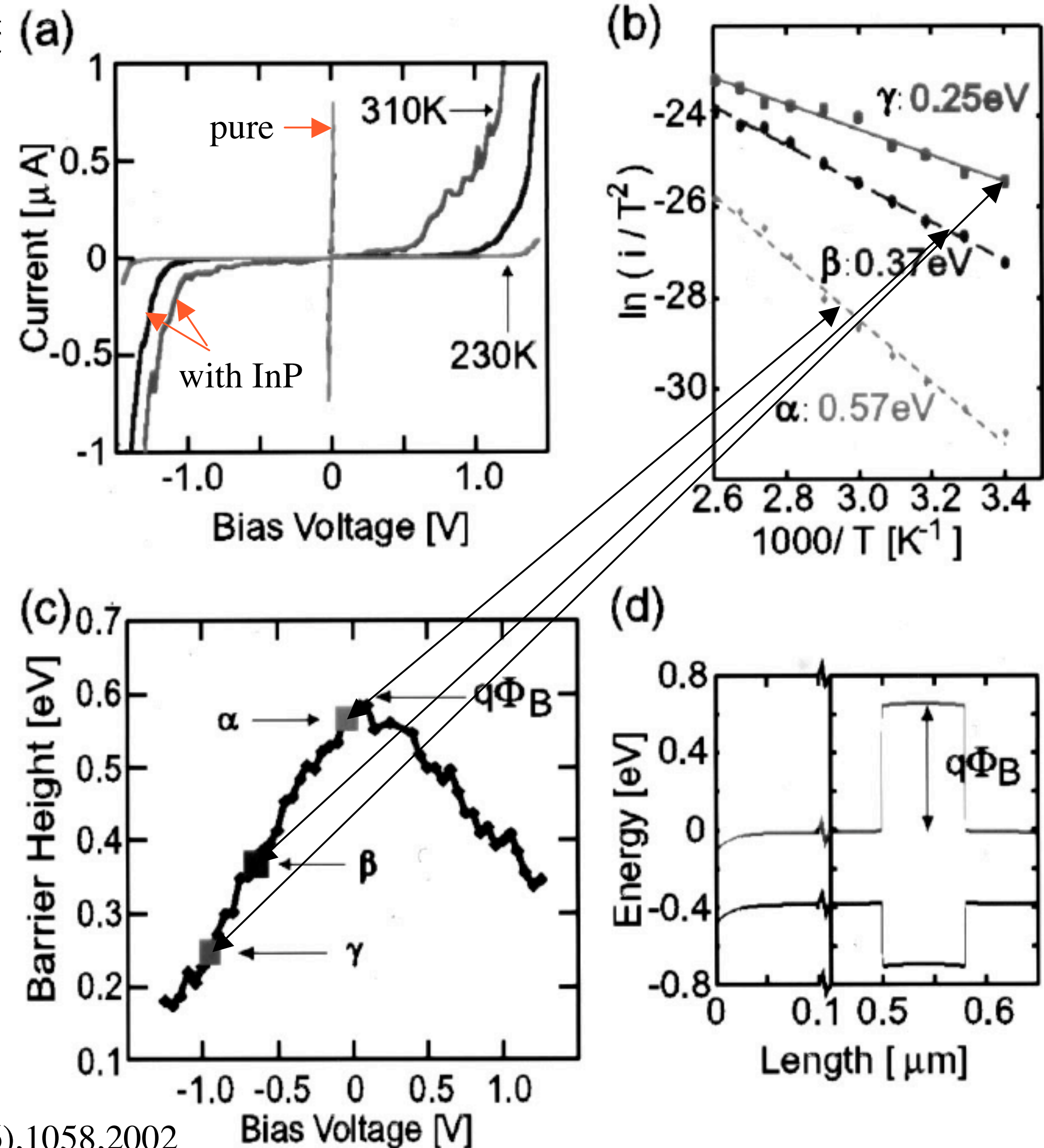
I-V Characteristic of InAs Wire with InP Barrier

a) I-V curves through pure InAs and InAs/InP wire in comparison. Strong current increases are a result from the barrier height reduction due to the applied bias.

b) Current depends on temperature: $I=const*T^2*exp[-q*\Phi_B/kT]$. Plot shows that Φ_B varies depending on the applied bias (voltages see c). Note $ln(I/T^2)$ vs. 1/T plot; Φ_B is extracted from slope.

c) Barrier height vs.bias voltage. Extrapolation to zero bias yields 0.6eV barrier height, which is close to the bulk heterojunction value.

d) Band line-up of InAs/InP heterojunction; ~0.6 eV conduction band barriers.



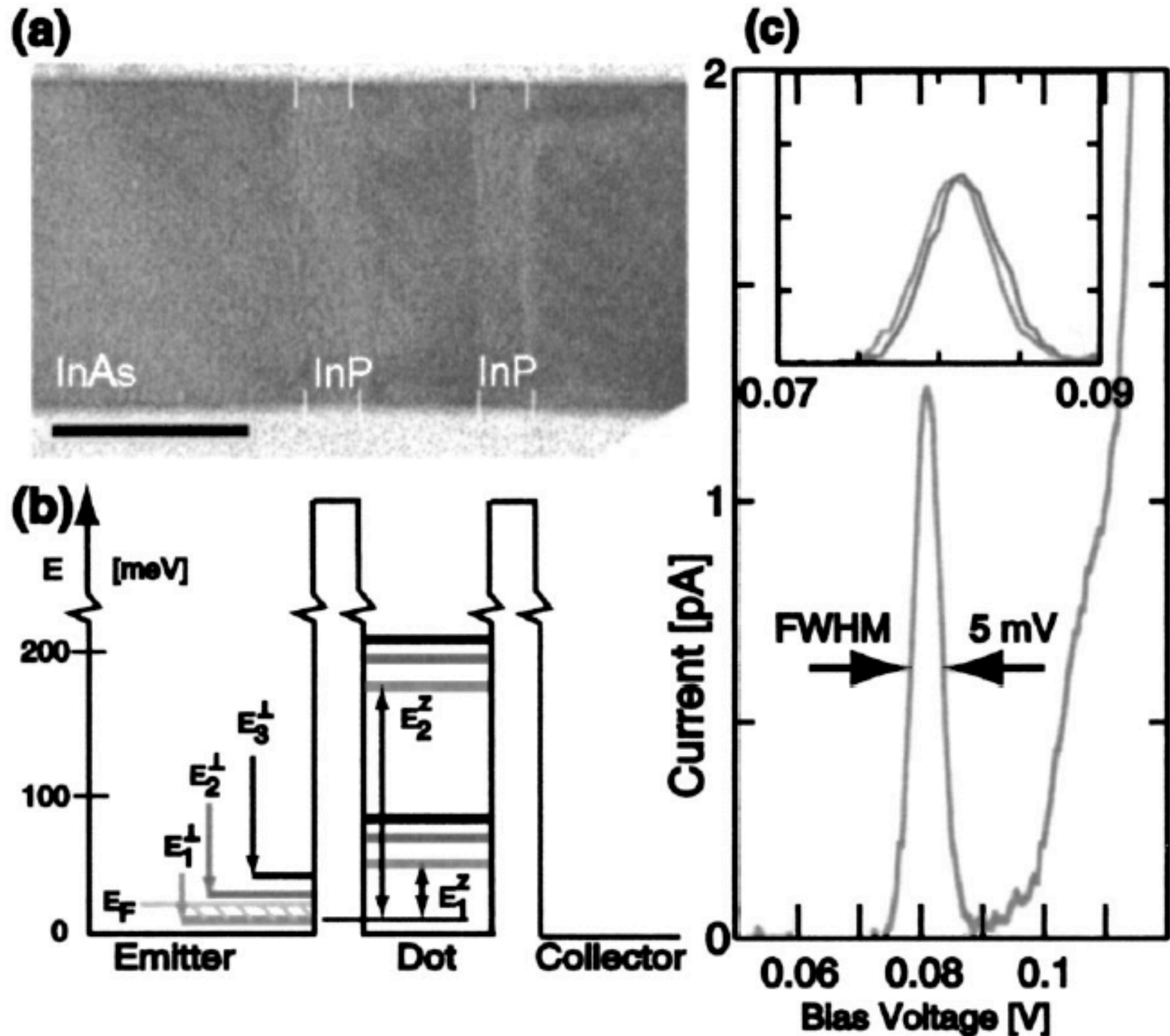
From: M.T.Björk et al. Appl.Phys.Lett. 80(6),1058,2002

Resonant Tunneling InAs/InP Device

a) 5 nm wide InP barriers in InAs. 15 nm wide InAs quantum dot in between.

b) Band diagram with electronic states. InAs is n-type; Fermi energy lies above E_1, i.e. E_1 is the only occupied state in the emitter. On the dot the states are split due to the different z-direction and transversal quantization. The smallest energy barrier is E_1^z.

c) I-V curve through wire. Current is zero below 70 mV applied bias. Sharp peak corresponds to tunneling through E_1^z. Insert shows repeat measurements.



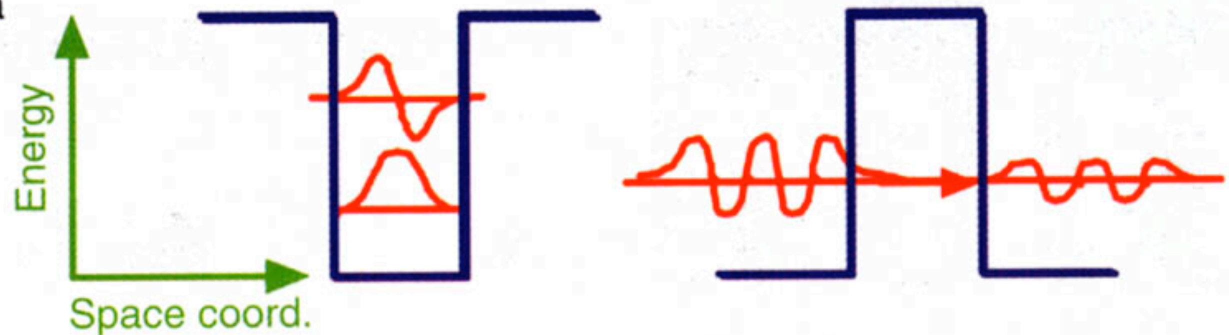
From: M.T. Björk et al. Appli.Phys.Lett. 81(23), pp.4458-61,2002

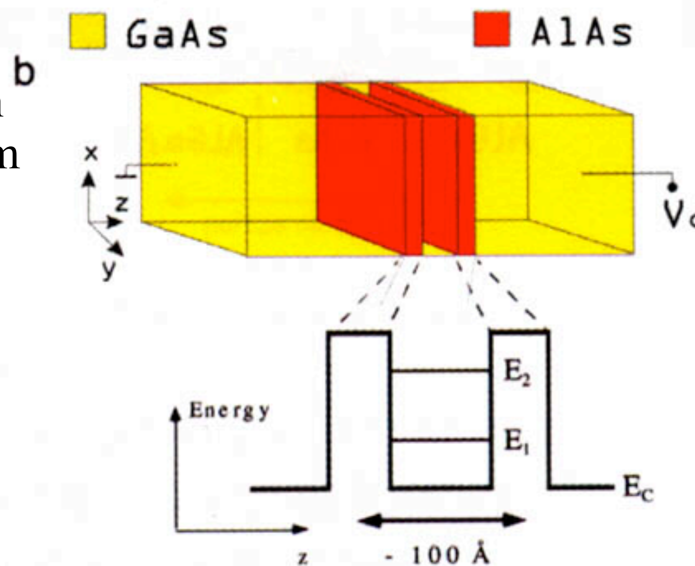
Quantum Dot Devices Schematic

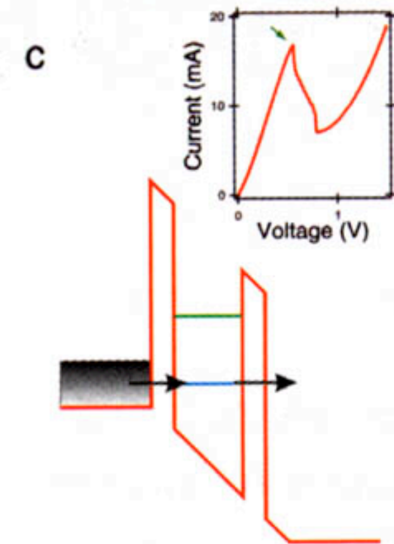
a) (left) Confinement of electrons in potential well results in discrete states. (right) Electron can tunnel through potentiaal barriers. Their energy is unaffected, only the amplitude of the wave function changes.

b) Heterojunctions between materials having different band gaps result in potential barriers. This can be used to prepare quantum dot devices.

c) When a SD bias is applied electrons tunnel through single states on the dot as they become available. Current spikes result.



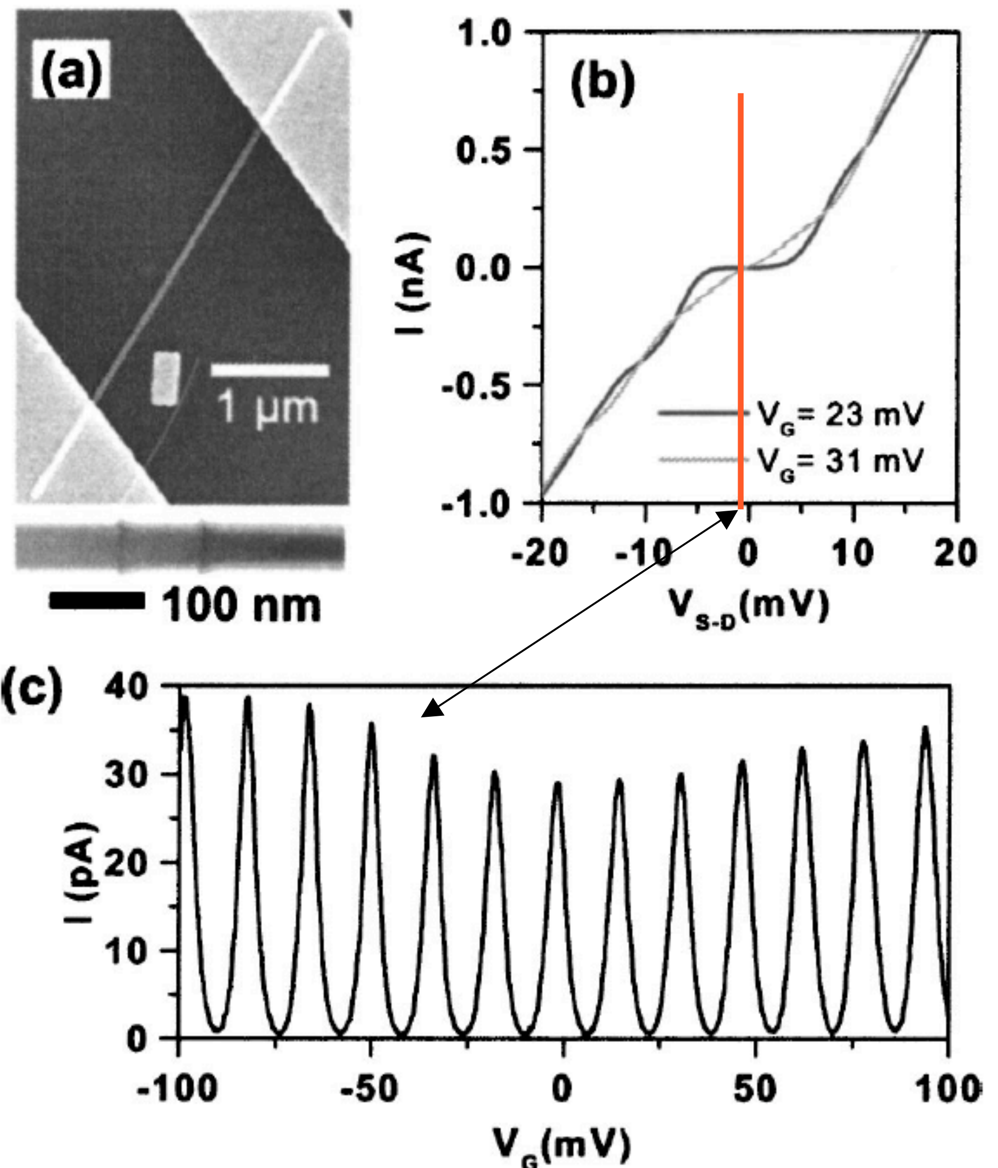




From: L.Samuelson, Materials Today 6(10), pp.22-31,2003

Effects of 80 nm Long InAs Quantum Dot

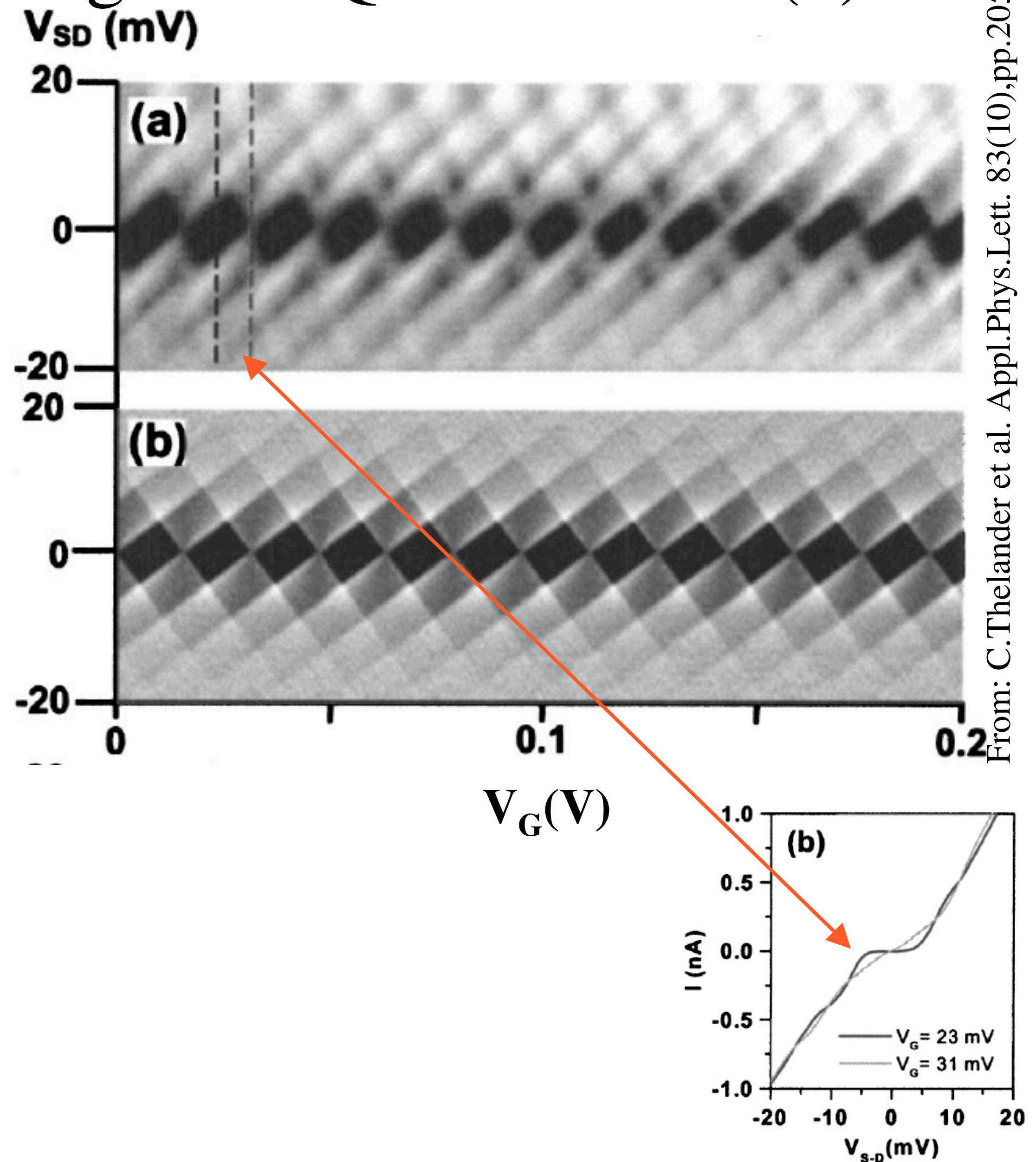
- Longer InAs section in wire results in more closely spaced energy states in the dot, i.e. many more peaks are being seen in I/V_G curve.
- (a) shows contacted wire between EBL contacts.
- (b) I/V_{SD} curves across the wire. Depending on bias applied to the wafer backside (gate) voltage V_G different “wiggles” (representing energy states that are being tunneled through) appear.
- (c) I/V_G curves at V_{SD}=0.5 mV. Note the pA scale.



From: C.Thelander et al. Appl.Phys.Lett. 83(10),pp.2052-55,2003

Effects of 80 nm Long InAs Quantum Dot (2)

- "Stability Plot" shows I/V_{SD} curves for whole V_G range. Gray scale corresponds to absolute current (black is zero, white ±1 nA).
- The dotted lines correspond to the two curves in the graph.
- Top plot: data
- Bottom plot: simulation



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